EXPRESS MAIL NO. EL872099960US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Leonard Forbes	Attorney Docket No.:	501268.01
Filed	: Concurrently Herewith	Examiner	: Not Yet Assigned
Title	: APPARATUS AND METHOD FOR SPLIT TRANSISTOR MEMORY HAVING IMPROVED ENDURANCE		

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97 through 1.98, applicant wishes to make known to the Patent and Trademark Office the references set forth on the attached form PTO-1449 (copies of the cited references, as required under 37 C.F.R. § 1.98, are enclosed). Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicant's duty to disclose all information he is aware of which is believed relevant to the examination of the above-identified application, applicant believes that his invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Respectfully submitted,

DORSEY & WHITNEY LLP

Steven H. Arterberry
Registration No. 46,314

SHA:jmw

Enclosures:
Postcard
Form PTO-1449
Cited References (4)

1420 Fifth Avenue, Suite 3400
Seattle, WA 98101
Telephone (206) 903-8800
Facsimile (206) 903-8820

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 501268.01	APPLICATION NO. Not Yet Assigned
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) Leonard Forbes	
		FILING DATE Concurrently herewith	GROUP ART UNIT Not Yet Assigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AK							
	AL							

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AM	Cappelletti, P. et al., "Failure Mechanisms of Flash Cell in Program/Erase Cycling", *IEEE*, 1994, IEDM-94, pp. 291-294.
	AN	Guan, Huinan et al., "On Scaling of SST Split-Gate Flash Memory Technologies", Department of Electrical and Computer Engineering, University of California, Irvine, Final Report 1998-1999 for MICRO Project 98-080.
	AO	Pavan, Paolo et al., "Flash Memory Cells – An Overview", *Proceedings of the IEEE*, Vol. 85, No. 8, August 1997, pp.1248-1271.
	AP	Seo, Jin-ho et al., "Charge-to-Breakdown Characteristics of Thin Gate Oxide and Buried Oxide on SIMOX SOI Wafers", *Journal of the Electrochemical Society*, Vol. 144, No. 1, January 1997, pp. 375-378.

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).